IN THE SPECIFICATION:

Please amend the Specification at page 32, lines 1-9, as follows:

Fig. 12 illustrates a processor consistent with the present invention. Processor 1110 may comprise one or more digital coefficient information obtaining components 1205 (though digital coefficient information can also be obtained by means external to the processor, such as via input/output device 1120, either alone or in combination with processor 1110), one or more motion vector determining components 1240, one or more memory management units (MMU) 1210, one or more processor element arrays 1220, and one or more accumulator units 1230. Processor element array 1220 may comprise an array of processor elements 1225. Processor elements 1225 may comprise, for example, a subtraction and adder units for calculating the SAD between the blocks. MMU 1210 may be used to buffer the data for processor element array 1220. Accumulator unit 1230 may be, for example, an adder unit that adds the outputs from processor elements 1225.